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Advanced Digital Power Solutions  Digital Signal Controller-Based Digital Power Supply

PZ307

Charlie Wu
Senior System & Application Engineer
Abstract

Learn about the emerging technology of digital power conversion as it applies to the markets of Switched-mode Power Supplies (SMPS), and Renewable Energy Converter. This class provides a technical overview of applications as well as hardware and software implementation based on Freescale 56800E Digital Signal Controller.
Emerging Technology in Digital Power Converters
Where Is Digital Power Conversion Applied?

► “Digital power Conversion” is a power system that is controlled by digital circuits, in much the same way as analog circuits, to monitor, supervise, communicate and control looping. A fully digitally controlled power system includes both digital control and digital power management.

► Digital Control
  • The control feedback or feed-forward loop, which is controlled by the digital circuit or programmable controller, regulates the output of the power system by driving the power switch duty cycle using pulse width modulation techniques.
  • The control circuits combine A/D conversion, Pulse Width Modulation, and Communication interfaces, operating entirely or mostly in digital mode.

► Digital Power Management
  • A Digital circuit or programmable controller provides the functions of configuration, tracking, monitoring, protection, supply sequencing, and communication with the environment.
Comparison of Analog and Digital Power Control System

Analog Control System With Digital Management

Full Digital Control System

DC Input
Voltage Ramp Network

Power Switch
PWM Generator

LC Filter
Analog Compensator Network

Current Ramp Network

Voltage

Scale

Power Switch

PWM Generator

LC Filter
Analog Compensator Network

Current

Scale

Fan

GPIO

Microcontroller

Serial Interface

A to D Converter

To Other Controllers

Voltage
Current
Temperature

Digital PW

DSP Controller

A to D Converter

GPIO

Serial Interface

To Other Controllers

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### Compare Digital Control To Analog Control

<table>
<thead>
<tr>
<th></th>
<th>Analog Control</th>
<th>Digital Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Circuit</td>
<td>Complex</td>
<td>Simple, Programmable, Integrated</td>
</tr>
<tr>
<td></td>
<td>Bulky</td>
<td></td>
</tr>
<tr>
<td>Flexibility</td>
<td>Bad</td>
<td>Good</td>
</tr>
<tr>
<td>Design Continuity</td>
<td>Bad</td>
<td>Good</td>
</tr>
<tr>
<td>Sample Mode</td>
<td>Continuous</td>
<td>Digitalization Error</td>
</tr>
<tr>
<td>Processing Course</td>
<td>Continuous</td>
<td>Control Delay</td>
</tr>
</tbody>
</table>
Analog Control vs. Digital Control
- Transient Response Comparison

**Traditional Analog control**
- Over voltage during load step-down
- Over current during load step-up

**Advanced Digital control**
- No OV and no OC during transient because of the smooth loop transition
- Output profile is programmable

**Constant Voltage**
- No OV and no OC during transient because of the smooth loop transition

**Constant Power**
- Over current during load step-up

**Power Fold Down**
- Over voltage during load step-down

**Constant Current**
Digital vs. Analog Control Loop

A typical control loop implemented by an analog circuit

\[
K \frac{A_0 + A_1 S + A_2 S^2 + A_3 S^3 + A_4 S^4}{B_0 + B_1 S + B_2 S^2 + B_3 S^3 + B_4 S^4}
\]

Power stage

\[
\frac{\kappa(1 + \gamma S)}{1 + \alpha S + \beta S^2}
\]

Nonlinear compensation

Adaptive compensation

Operation condition

A digital control loop implemented by Digital Signal Controller (DSC)

Benefit of digital control:
1) Optimize feedback loop to meet application requirements
2) Runtime changes to compensation parameters according to operating conditions
Real-time Digital System Model

Analog signal → A/D convert → Signal processing → D/A convert → Analog signal

- Quick
- High precision
- Quick
- Real time
Quantization Effects  
- PWM resolution

PWM resolution = PWM clock ÷ PWM Switching Frequency

Assume 1:
PWM clock = 32Mhz; PWM Switching Frequency = 250KHz
PWM Resolution = 32,000,000 ÷ 250,000
= 128 (2^7 or 7 bit)

Assume 2:
PWM clock = 96Mhz; PWM Switching Frequency = 250KHz
PWM Resolution = 96,000,000 ÷ 250,000
= 384 (1.5×2^8 or 8.5 bit)

If DC bus voltage is 300VDC, each bit represents:
7 bit PWM resolution: 48VDC ÷ 128 = 0.375V (0.78% accuracy)
8.5 bit PWM resolution: 48VDC ÷ 348 = 0.138V (0.29% accuracy)

The second Assumption yields higher PWM resolution, less Voltage variation per bit change. So the voltage ripple on output will be smaller.
Quantization Effects
- ADC Resolution and Speed

Analog signal Input → A/D convert → Signal processing → D/A convert → Analog signal Output

Low ADC Resolution → Signal Reconstruction

High ADC Resolution And Speed → Signal Reconstruction

Higher Signal Distortion
Lower Signal Distortion
**Increase PWM resolution: Digital Dithering Technique**

*Dither* is a form of noise, or erroneous signal or data which is deliberately added to sample data for the purpose of minimizing quantization error.

- The quantization error is a repeatable error as the value repeat.
- Digital dithering is a system wherein the error does not repeat as the value repeat.
- In digital power system, digital dithering technique will reduce the PWM quantization error.
- **If a digital PWM module can not output a value that matches the Control Loop’s calculated value, the control loop will dither between the two closest values to obtain the desired result.**

![Diagram showing PWM waveform with and without dithering.](image)

**Calculated PWM Duty Value = 49.5**

**Without Dithering**

- Voltage At Point A
- Current At Point B

**With Dithering:**

- PWM dithers Between 49 & 50

**PWM Duty Cycle** = \[
\frac{\text{PWM Duty Value}}{\text{Modulo}}
\]
Transfer Function Of Control Loop

- $V^*_o$ is the reference; $V_o$ is the output; $K_{vs}$ is the feedback gain.
- Control loop includes a PID controller and a power stage model.
- PID controller is a dynamic error regulator.
Control Law Processor - PID Controller
(Proportional-Integral-Derivative)

- **Continuous (Analog) Expression**

\[ M(t) = K_p e(t) + K_i \int e(t) \, dt + K_d \frac{d}{dt} e(t) \]  

\[ e(t) = X_i(t) - X_f(t) \]  

Where \( e(t) \): Error signal; \( K_p \): Proportional Gain; \( K_i \): Integral Gain; \( K_d \): Derivative Gain

- **Difference (Digital) Expression**

\[ m(n) = K_p e(n) + K_i \sum_{i=0}^{n} e(i) \Delta t + K_d \frac{e(n) - e(n-1)}{\Delta t} \]

\[ m(n) = m(n-1) + K_p [e(n) - e(n-1)] + K_i e(n) \Delta t + K_d \left[ \frac{e(n) - e(n-1)}{\Delta t} - \frac{e(n-1) - e(n-2)}{\Delta t} \right] \]
Design Of Control Feedback Loop In Digital Domain

PID Regulating Loop

Conversion To Z – Transformation

\[ z[e(n-1)] = z^{-1} E(z) \] \& \[ z\left[ \sum_{i=1}^{n} e(n) \right] = \frac{E(z)}{1 - z^{-1}} \]

From Equation (4)

\[ G_{VEA}(z) = \frac{M(z)}{E(z)} = K_{pv}^* + \frac{K_{iv}^*}{1 - z^{-1}} + K_{id}^* (1 - z^{-1}) \]  

(5)

Where : \[ K_{pv}^* = K_p \] ; \[ K_{iv} = K_i \times \Delta t \] ; \[ K_{id} = K_d \div \Delta t \]

Digital PID Controller

![Digital PID Controller Diagram]
Design Of Control Feedback Loop In Digital Domain

Model Of Power Stage Transfer Function

\[
G_v(S) = \frac{\tilde{v}_o}{\tilde{v}_{vo}} = \frac{K}{SCV_o}
\]

\(\tilde{V}_o\) and \(\tilde{V}_{vo}\) are values of output and loop output

\[
G_{vh}(z) = Z(G_{vh}(S)) = (1 - z^{-1})Z\left[\frac{G_v(S)}{S}\right] = \frac{K \cdot T_s}{CV_o(z - 1)}
\]

✓ Power stage Z-transformation function
PID Parameter Design For Feedback Loop Control

Measurement criteria for a stable closed loop system

- Phase margin should be greater than 45° at open loop cross frequency

\[ \angle G_{v\text{-open}}(e^{j \omega_c T_s}) > -180^\circ + 45^\circ \text{ at where } \left| G_{v\text{-open}}(e^{j \omega_c T_s}) \right| = 1 \]

- Gain margin should be greater than one at the frequency where the phase shift is -180°

\[ \frac{1}{\left| G_{v\text{-open}}(e^{j \omega_c T_s}) \right|} > 1 \text{ at where } \angle G_{v\text{-open}}(e^{j \omega_c T_s}) = -180^\circ \]
Benefits of Digital Power

- **Free from** the effects of **component tolerance**, parametric drift, aging, etc
- **Configurable** feedback loop **structure** for specific application requirements
- **Adaptive control** to meet changing operating conditions
- **Flexible** Pulse Width **Waveform-generation** module
- **Programmable relationships** among **PWM** outputs
- **Upgradeable** with new features **without hardware** changes
- **Retainable** operational **data** for diagnostic and record keeping
- **Diverse communications** capabilities
- **Reduced** component count - and **cost**
- **Higher** power density due to over all **integration**
- **Shorter R&D cycle**, fewer turns of board prototyping
- **Portable Projects** for faster reuse
- **Defendable firmware** - protects IP and differentiating technology
Typical DSP-based AC/DC Converter

- **Primary DSP**
  - AC sensing
  - LED
  - Thermal
  - Fan
  - A/D
  - PWM
  - PFC

- **Secondary DSP**
  - AC sensing
  - LED
  - Thermal
  - Fan
  - A/D
  - PWM
  - Current sharing
  - OV/OC detection
  - System info / control
  - Discrete status report
  - RS485 / I2C (communication)

- **PFC**
- **Isolated DC/DC**
Production Overview
Controller Continuum

High
- MobileGT™ MPC5200
- ColdFire® MCF5xxx family
- MPC5xx family based on Power Architecture™ Technology
- i.MX family based on ARM® technology

Upper Mid
- ColdFire® MCF5xxx family
- 56F83xx/81xx hybrid family
- 568xx hybrid family

Mid
- 56F800 hybrid family
- 56F801x hybrid family
- HCS12 16-bit family

Low
- HCS08 LVLP 8-bit family
- HC08 8-bit family
- RS08 8-bit family

In Addition, Freescale also offers……

Host & Communications Processors based upon the Power Architecture™ Technology

- SMAC
- 802.15.4
- Zigbee
- Accelerometers
- Pressure
- Proximity
- Motion control
- Power mgmt
- QUICC supply
- I/O expansion

In Addition, Freescale also offers……
What is Digital Signal Controller

- Specialized microprocessor whose architecture contains a core engine capable of competitively performing both microcontroller and digital signal processor functionalities
- Core processing capability applicable to many types of system solutions
- Common basic features:
  - MAC, single instruction cycle allowing several memory accesses, address generation units, algorithms for efficient looping
- Specialized cost effective, high performance on-board interfaces utilized in implementing embedded control applications:
  - PWM; multifunction timer; high speed ADCs; DACs; Comparators; SCIs (UART); SPIs; CANs and I2Cs, etc.
- Embedded nonvolatile memory:
  - Flash memory, ROM or EEPROM
- Easy to use development tools
56800/E Family Combining Signal Processing and Controller Functionality

Traditional Microcontroller

- Designed for Controller Code
- Compact Code Size
- Easy to Program
- Inefficient Signal Processing

Traditional DSP Engine

- Designed for DSP Processing
- Designed for Matrix Operations
- Complex Programming
- Less Suitable for Control

- Instructions Optimized for Controller Code, DSP, Matrix Operations
- Compact Assembly and “C” Compiled Code Size
- Easy to Program
- Additional MIPS Headroom and extended addressing space
### DSP56800E Core Features

<table>
<thead>
<tr>
<th>CPU</th>
<th>MIPS</th>
<th># Interrupt Priorities</th>
<th>Registers</th>
<th>Data Types</th>
<th>Program Memory Adr Space</th>
<th>Data Memory Adr Space</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP56800E</td>
<td>120 from RAM</td>
<td>5</td>
<td>7 Data</td>
<td>8-bit, 16-bit</td>
<td>4 MB</td>
<td>32 MB</td>
<td>Fully Synthesizable and Scanable</td>
</tr>
<tr>
<td></td>
<td>60 from Flash</td>
<td></td>
<td>8 Address</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 56800/E MCU Functionality
- True Software Stack and Pointer
- 16-bit Program Word
- 20 Addressing Modes and Atomic Read-Modify-Write Instructions
- General Purpose Register Files and Orthogonal Instructions to Data and Address Register Files
- Full Set of Bit and Bitfield Manipulation Instructions and 16- and 32-bit Shifting
- Superfast Interrupt

### 56800/E DSP Functionality
- Multiplier - Accumulator (MAC)
- Single And Dual Parallel Move Instructions
- No Overhead Hardware Looping
- Nested Looping Capability
- Modulo arithmetic (For Circular Buffers)
- Integer and Fractional Arithmetic Support
- Nested Interrupt with HW priority
- Fast Interrupt Support
# DSP56800E General Purpose Registers

## Data Arithmetic Logic Unit

### Data Registers

<table>
<thead>
<tr>
<th></th>
<th>A2</th>
<th>A1</th>
<th>A0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>B2</td>
<td>B1</td>
<td>B0</td>
</tr>
<tr>
<td>C</td>
<td>C2</td>
<td>C1</td>
<td>C0</td>
</tr>
<tr>
<td>D</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>

### Y Registers

- Y1
- Y0
- X0

## Address Generation Unit

### Pointer Registers

- R0
- R1
- R2
- R3
- R4
- R5
- N
- SP

### => 8 Address Registers

## Program Control Unit

### Program Counter

- PC

### Operating Mode and Status

- OMR
- SR

### => 7 Data Registers

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Registers with Dedicated Functionality

PROGRAM CONTROL UNIT

=> HW Looping
Nested 2 Deep

ADDRESS GENERATION UNIT

=> Shadows

=> Modulo
Addressing

=> Fast
Interrupt
=> R0, R1, N, and M01 registers are shadowed
Mapping the Architecture to DSP Algorithms

Common Operation in DSP

MAC X0, Y0, A  X:(R4)+, Y1  X:(R3)+, C
Arithmetic Op  1st Read  2nd Read

Operations Performed:
• Multiply-Accumulate
• 3 Memory Accesses
• 2 Address Additions

Instruction Fetch:
- PAB - 21 bits
- PDB - 16 bits

1st Data Access:
- XAB1 - 24 bits
- CDBR - 32 bits

2nd Data Access:
- XAB2 - 24 bits
- XDB2 - 16 bits
Data ALU - General Purpose Register File

**Conventional DSP**

SRC1 → DATA ALU

SRC2 → DATA ALU

A1 → A0
B1 → B0

INC, DEC, ASL, ASR
ADD, etc.

“Accumulator Based”

**DSP56800E**

<table>
<thead>
<tr>
<th>A2</th>
<th>A1</th>
<th>A0</th>
</tr>
</thead>
<tbody>
<tr>
<td>B2</td>
<td>B1</td>
<td>B0</td>
</tr>
<tr>
<td>C2</td>
<td>C1</td>
<td>C0</td>
</tr>
<tr>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Y1</td>
<td>Y0</td>
<td></td>
</tr>
<tr>
<td>X0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

INC.W, DEC.W
ASL, ASR
FFF, FFF

ADD, etc.
FFF, FFF

“GP Register File”
Powerful Set of Addressing Modes

- **Indirect**
  - X:(Rn) No Update
  - X:(Rn)+ Post Increment
  - X:(Rn)- Post Decrement
  - X:(Rn)+N Post Update by Register

- **Indexed**
  - X:(Rn+x) Indexed: 3-bit Offset
  - X:(SP-xx) Indexed: 6-bit Offset
  - X:(Rn+xxxx) Indexed: 16-bit Offset
  - X:(Rn+xxxxx) Indexed: 24-bit Offset
  - X:(Rn+N) Indexed: By a Register

- **Immediate**
  - #x 5-bit “Long” Constant
  - #xx 6-bit Loop Ct
  - #xx 7-bit Short
  - #xxxx 16-bit
  - #xxxxxxxx 32-bit

- **Absolute**
  - X:aa 6-bit Absolute Short
  - X:<<pp 6-bit Peripheral Direct
  - X:xxxx 16-bit Absolute
  - X:xxxxx 24-bit Absolute

- **Other**
  - DDDDD Register Direct
  - * Inherent

Supports 8, 16, 32-bits
Supports Modulo Arithmetic
Embedded System Trend

- Component Usage
- Manufacturing cost

- Feature Integration
- Operating Frequency

- Technology Geometry
- Power Consumption

2000’s

- 0.35u
- 0.25u
- 0.18u
- 0.90nm

Controller Cost

2010’s

- 0.65nm
High Performance 56F8300 Solutions
56F836x/56F835x/56F834x/56F832x 60MHz/60MIPS

- 60 MIPS Performance
- Program Memory
  - Up to 512Kbytes FLASH
  - Up to 4Kbytes RAM
  - Up to 32Kbytes BootFLASH™
- Data Memory
  - Up to 32Kbytes FLASH
  - Up to 32Kbytes RAM
- Serial Ports: SCIs and SPIs, CANs
- Quad, 4 channel, 12-bit ADC
- Dual 6-Output PWM Modules
- Synchronization between PWM and ADC
- Up to Sixteen multifunction 16-bit Timers
- External Memory Interface
- COP/Watchdog Timer
- Up to 76 GPIO – Versatile pin usage
- System Clock Generator
- On-chip temperature sensor
- On-chip Voltage Regulator and Power Supervisor
- Vectored Interrupt Controller
- JTAG/OnCE™ Debug Port

- Packages: 48/64/128/144/160LQFP and 160 MBGA
- Derivatives: 23 devices

Key Control Peripherals
### 56F8300 Series (1 of 2)

<table>
<thead>
<tr>
<th>Feature</th>
<th>56F8322</th>
<th>56F8323</th>
<th>56F8335</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Performance</strong></td>
<td>60MHz/MIPS</td>
<td>60MHz/MIPS</td>
<td>60MHz/MIPS</td>
</tr>
<tr>
<td><strong>Temp. Range</strong></td>
<td>(-40, +125)°C</td>
<td>(-40, +125)°C</td>
<td>(-40, +125)°C</td>
</tr>
<tr>
<td><strong>Voltage (Core / I/O)</strong></td>
<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
</tr>
<tr>
<td><strong>On-Chip Flash</strong></td>
<td>48KB</td>
<td>48KB</td>
<td>80KB</td>
</tr>
<tr>
<td><strong>Program Flash</strong></td>
<td>32KB</td>
<td>32KB</td>
<td>64KB</td>
</tr>
<tr>
<td><strong>Data Flash</strong></td>
<td>8KB</td>
<td>8KB</td>
<td>8KB</td>
</tr>
<tr>
<td><strong>Boot Flash</strong></td>
<td>8KB</td>
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<td>8KB</td>
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<tr>
<td><strong>On-Chip RAM</strong></td>
<td>12KB</td>
<td>12KB</td>
<td>12KB</td>
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<tr>
<td><strong>Program RAM</strong></td>
<td>4KB</td>
<td>4KB</td>
<td>4KB</td>
</tr>
<tr>
<td><strong>Data RAM</strong></td>
<td>8KB</td>
<td>8KB</td>
<td>8KB</td>
</tr>
<tr>
<td><strong>Flash Security</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td><strong>Ext. Memory Interface</strong></td>
<td>-</td>
<td>-</td>
<td>-</td>
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<tr>
<td><strong>Internal Voltage Regulator</strong></td>
<td>On-Chip</td>
<td>On/Off-Chip</td>
<td>On/Off-Chip</td>
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<tr>
<td><strong>On-Chip Relaxation Osc.</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td><strong>16-bit Timers</strong></td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td><strong>Quadrature Decoder</strong></td>
<td>1 x 4ch</td>
<td>1 x 4ch</td>
<td>2 x 4ch</td>
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<tr>
<td><strong>PWM</strong></td>
<td>1 x 6ch</td>
<td>1 x 6ch</td>
<td>2 x 6ch</td>
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<tr>
<td><strong>PWM Fault Input</strong></td>
<td>1</td>
<td>3</td>
<td>4 + 4</td>
</tr>
<tr>
<td><strong>PWM Current Sense Pins</strong></td>
<td>0</td>
<td>3</td>
<td>3 + 3</td>
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<tr>
<td><strong>12-bit ADC</strong></td>
<td>2 x 3ch</td>
<td>2 x 4ch</td>
<td>4 x 4ch</td>
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<tr>
<td><strong>Temperature Sensor</strong></td>
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<td>Optional</td>
<td>Optional</td>
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<tr>
<td><strong>CAN</strong></td>
<td>FlexCAN</td>
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<tr>
<td><strong>SCI (UART)</strong></td>
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<td><strong>SPI (Synchronous)</strong></td>
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<tr>
<td><strong>GPIO (Ded./Shrd/Tot)</strong></td>
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<td>0 / 27 / 27</td>
<td>21 / 28 / 49</td>
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<td><strong>JTAG/EOnCE</strong></td>
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<td>Yes</td>
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<td><strong>Package</strong></td>
<td>48LQFP</td>
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<td>128LQFP</td>
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## 56F8300 Series (2 of 2)

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<tr>
<th>Feature</th>
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<th>56F8346</th>
<th>56F8347</th>
<th>56F8355</th>
<th>56F8356</th>
<th>56F8357</th>
<th>56F8355</th>
<th>56F8366</th>
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<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
<td>2.5/3.3V</td>
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<td><strong>On-Chip Flash</strong></td>
<td>144KB</td>
<td>144KB</td>
<td>144KB</td>
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<td>280KB</td>
<td>560KB</td>
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<td><strong>Program Flash</strong></td>
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<td>128KB</td>
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<td>256KB</td>
<td>256KB</td>
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<td><strong>Data Flash</strong></td>
<td>8KB</td>
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<td><strong>Boot Flash</strong></td>
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<td>8KB</td>
<td>8KB</td>
<td>16KB</td>
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<td>12KB</td>
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<td>4KB</td>
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<tr>
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<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<td><strong>Ext. Memory Interface</strong></td>
<td>-</td>
<td>Yes</td>
<td>Yes</td>
<td>-</td>
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<td>-</td>
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<td>No</td>
<td>No</td>
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<td><strong>16-bit Timers</strong></td>
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<td><strong>Quadrature Decoder</strong></td>
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<td><strong>PWM</strong></td>
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<td>2 x 6ch</td>
<td>2 x 6ch</td>
<td>2 x 6ch</td>
<td>2 x 6ch</td>
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<td><strong>PWM Fault Input</strong></td>
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<td>3 + 4</td>
<td>3 + 4</td>
<td>4 + 4</td>
<td>3 + 4</td>
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<td>4 + 4</td>
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<tr>
<td><strong>PWM Current Sense Pins</strong></td>
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<td>4 x 4 ch</td>
<td>4 x 4 ch</td>
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<td>FlexCAN</td>
<td>FlexCAN</td>
<td>FlexCAN</td>
<td>FlexCAN</td>
<td>FlexCAN</td>
<td>FlexCAN (2)</td>
<td>FlexCAN (2)</td>
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<td>2</td>
<td>2</td>
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<td><strong>SPI (Synchronous)</strong></td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
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<td>21/ 28 / 49</td>
<td>0 / 62 / 62</td>
<td>0 / 76 / 76</td>
<td>21/ 28 / 49</td>
<td>0 / 62 / 62</td>
<td>0 / 76 / 76</td>
<td>21/ 28 / 49</td>
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<tr>
<td><strong>JTAG/EOnCE</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<td><strong>Package</strong></td>
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<td>144LQFP</td>
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<td>160LQFP</td>
<td>128LQFP</td>
<td>144LQFP</td>
<td>160LQFP</td>
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</tbody>
</table>
56F8000 Series

- New platform to address the needs of cost sensitive applications requiring a **high performance** 16-bit solution

- Extended Temperature
  - -40°C to +105°C
  - -40°C to +125°C

- Low pin count, easy to manufacture with packages

- **Aggressive** price points
Cost Effective 56F8000 Solutions
56F8011/56F8013/56F8014

- 32 MIPS Performance
- 12K -16 K Bytes Program FLASH
- 4 K Bytes Program/Data RAM
- Tunable Internal Relaxation Oscillator
- Software Programmable Phase Locked Loop
- Up to 96 MHz Peripherals – Timers and PWMs
- Up to 6-Output PWM Module with up to 4 Programmable Fault Inputs
- Selectable PWM frequency for each complementary PWM signal pair
- Two 12-bit ADCs with up to 8 Inputs , 1.125us conversion rate
- Synchronization between PWM and ADC
- Four 16-bit General Purpose Programmable Timers
- Computer Operating Properly Timer
- Serial Ports: SCI, SPI, I2C
- Up to 26 GPIOs – Versatile pin usage
- Low Power Consumption – 59mA Max and .026mA Min
- JTAG/EOnCE™ Debug Port
- Industrial & Automotive temp
- Cost Effective
32 MHz/32 MIPS 56800E Core
3.0-3.6V Operation
32K-64K Bytes Program FLASH
4K-8K Bytes Program/Data RAM
Flash security
Tunable Internal Relaxation Oscillator
Software Programmable Phase Locked Loop
Up to 96 MHz Peripherals – Timers and PWMs
6 Output PWM Module with 4 Programmable Fault Inputs
Selectable PWM frequency for each complementary PWM signal pair
Two 12-bit ADCs with up to 16 Inputs, 1.125us conversion rate
Up to Two 12-bit Digital to Analog Converters
Two Analog Comparators
Synchronization between PWM and ADC
4 or 8 16-bit General Purpose Programmable Timers
1 or 3 Programmable Interval Timers (PIT)
Computer Operating Properly Timer
2-Queued Serial Communications Interface
2-Queued Serial Peripheral Interface
Optional MSCAN
I²C Communications Interface
Up to 53 GPIOs – Versatile pin usage
JTAG/EOnCE™ Debug Port
Lead Free “Green” Packages
Industrial & Automotive temp
## 56F8000 Series Feature Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>56F8011</th>
<th>56F8013</th>
<th>56F8014</th>
<th>56F8023</th>
<th>56F8025</th>
<th>56F8036</th>
<th>56F8037</th>
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<tbody>
<tr>
<td><strong>Performance</strong></td>
<td>32MHz/MIPS</td>
<td>32MHz/MIPS</td>
<td>32MHz/MIPS</td>
<td>32MHz/MIPS</td>
<td>32MHz/MIPS</td>
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<td>3.0V - 3.6V</td>
<td>3.0V - 3.6V</td>
<td>3.0V - 3.6V</td>
<td>3.0V - 3.6V</td>
<td>3.0V - 3.6V</td>
<td>3.0V - 3.6V</td>
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<td><strong>Program/Data Flash</strong></td>
<td>12KB</td>
<td>16KB</td>
<td>16KB</td>
<td>32KB</td>
<td>32KB</td>
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<td>64KB</td>
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<tr>
<td><strong>Program/Data RAM</strong></td>
<td>2KB</td>
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<td>4KB</td>
<td>4KB</td>
<td>4KB</td>
<td>8KB</td>
<td>8KB</td>
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<td><strong>On Chip Relaxation Osc.</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<td>Yes</td>
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<td>Yes</td>
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<td>Yes</td>
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<td><strong>COP</strong></td>
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<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<td><strong>PWM</strong></td>
<td>1 x 6ch</td>
<td>1 x 6ch</td>
<td>1 x 5ch</td>
<td>1 x 6ch</td>
<td>1 x 6ch</td>
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<td><strong>12-bit ADCs</strong></td>
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<td>No</td>
<td>No</td>
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<td>No</td>
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<td><strong>Analog Comparator</strong></td>
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<td>No</td>
<td>No</td>
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<td>2</td>
<td>2 (Pinned out)</td>
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<td><strong>16-bit Timers</strong></td>
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<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>8</td>
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<td><strong>Prog. Interval Timers</strong></td>
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<td>No</td>
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<td>3</td>
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<td>35</td>
<td>39</td>
<td>53</td>
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<td>1</td>
<td>1</td>
<td>1</td>
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<td>1 - SCI</td>
<td>1 - SCI</td>
<td>1 - SCI</td>
<td>1 - QSCI</td>
<td>1 - QSCI</td>
<td>1 - QSCI</td>
<td>2 - QSCI</td>
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<td>1 - SPI</td>
<td>1 - SPI</td>
<td>1 - QSPI</td>
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<td>2 - QSPI</td>
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<td><strong>CAN</strong></td>
<td>JTAG/EOnCE</td>
<td>JTAG/EOnCE</td>
<td>JTAG/EOnCE</td>
<td>JTAG/EOnCE</td>
<td>JTAG/EOnCE</td>
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<td>JTAG/EOnCE</td>
<td>JTAG/EOnCE</td>
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<tr>
<td><strong>Package (V) - Industrial</strong></td>
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<td>32LQFP (.8p)</td>
<td>32LQFP (.8p)</td>
<td>32LQFP (.8p)</td>
<td>44LQFP (.8p)</td>
<td>48LQFP (.5p)</td>
<td>64LQFP (.5p)</td>
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</tbody>
</table>

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56F8000 Feature Highlights - Memory

- Up to 16K Bytes Flash memory
- Up to 4K Bytes Unified RAM
- On Chip Dual Harvard Architecture
- Programmable “Code Protection” feature
- Programmable “Code Security” feature
- Flash with 256 word page size enabling EEPROM emulation (HW & SW Support)
- Can program one word at a time
- Flash memory programmable via JTAG/OnCE interface or user defined programming (such as SPI, SCI)
- Flash Signature Calculator
- 32MHz operation for 56F80xx and 60Mhz operation for 56F83xx at 125°C
Pulse Width Modulator (PWM)

- Clock PWM up to 96Mhz
- Three complementary signal pairs or six independent signals or combinations
- Complementary channel operation
  - Separate Deadtime insertions for rising and falling edge
  - Separate top and bottom polarity control
- Edge-aligned or center-aligned signals
- 15-bits of resolution
- Half-cycle reload capability
- Asymmetric mode of operation (for phase shifting)
- Programmable integral reload rates (half to 16)
- Individually software-controlled PWM outputs
- ADC synchronization
- Up to 4 Programmable fault inputs
- PWM compare output polarity control
- 8 or 4 mA current source/sink
- Output Polarity Control
- Write protected registers
- Double-buffered PWM registers
- Wait/Debug mode operation
- Selectable PWM supply source for each complementary PWM signal pair (F8000family only)
  - PWM Generator
  - External GPIO
  - Internal timer channel
  - ADC conversion result, taking into account values setting ADC high and low limit register
• Fault inputs can independently monitor critical system parameters, and generate an interrupt when asserted.
• Each input is mappable to immediately disable any or all PWMs
• Each input is programmable to allow Automatic or Manual PWM restart
PWM Fault Decode and Automatic Clearing

*When Fault logic returns to logic 0, the PWM restart at beginning of the next half cycle.*
**56F8000 Feature Highlights - Quad Timers**

- Up to 96 MHz operation
- Four 16-bit general purpose up/down timers
- Individually programmable
  - Input capture trigger
  - Output compare capture
  - Selectable input clock source
  - Quadrature Decode
  - Pulse Generation
- Input pins are shareable within a timer module
- Each timer has separate prescaler
- Counters are pre-loadable
- Counters in module can be daisy-chained to yield longer counter lengths, up to 64-bits
- Up to 12 operating modes
- Timer outputs can generate PWM complementary pair output signals
Quad Timer: Simple Operating Modes

Stop Mode - Counter is inert. No counting will occur

Signed Count Mode – Counts primary input up or down based on polarity of secondary input

Edge Count Mode – Counts rising and falling edges (counting of simple encoder wheel)

Count Mode – Counts rising or falling edges (generating periodic interrupts, timing purposes)

Gated Count Mode - Counts primary input if secondary input is high (signal width measurement)

Cascaded Count Mode - Input is connected to the output of another (Great for large counts up to \(2^{34}\))
Triggered Count Mode – Start/Stop count of Primary input on rising edge of Secondary input.

One-Shot Mode - Provides timing delays
(ADC acquisition of new samples until a specified period of time has passed since the PWM sync signal occurred)
Quad Timer: Other Modes

Fixed Frequency PWM - Fixed frequency, variable duty cycle (driving PWM amplifiers)

Variable Frequency PWM - Variable frequency and duty cycle (driving PWM amplifiers)

Pulse Output Mode - Supports stepper motor systems and provides change of signal frequency and number of pulses

Quadrature Count Mode

• Counter will decode the primary and secondary external inputs as quadrature encoded signals
• Compare interrupts will signal commutation
Analog to Digital Converters

- 12-bit resolution
- Two ADCs per module
  - 6 to 8 Analog Inputs per module
  - Independent sampling frequency per ADC
- Sampling rate up to 1.78 million samples per second
  - Sequential: First 1.59us subsequent 1.125us
  - Simultaneous: 8 conversions in 4.48us
- Can be internally synchronized to a PWM reload event
- Simultaneous or sequential sampling
- Optional sample correction by subtracting a pre-programmed offset value
- 4 Interrupt types:
  - End of a scan, zero crossing, High/Low limit
  - High/Low Limits can control PWM outputs
- Signed or unsigned result
- Single-ended or differential inputs for all input pins with support for an arbitrary mix of input types
- Power savings modes
  - Explicit power down of all/part of ADC
  - Intelligent power savings mode: Auto wake-up
- Internal or External Voltage Reference

Note: 56F83xx conversion time:
- Sequential: First 1.7us subsequent 1.2ns
- Simultaneous: 8 conversions in 5.3us
Once

- The ADC starts to sample just one time whether you use the START bit or by a sync pulse. This mode must be re-armed by writing to the ADCR1 register again if you want to go capture another scan.

Triggered

- Sampling begins with every recognized START command or sync pulse.

Loop

- The ADC continuously take samples as long as power is on and the STOP bit has not been set.

Sequential Mode

- Sequential will sample SampleN one after another. Channel ANAx are sampled by ADCA and Channel ANBx are sampled by ADCB.

Parallel Mode

- Simultaneous: Parallel can sample SampleN from Group1 and SampleN from Group 2 at the same time.
- Independent:: ADCA and ADCB can operate independently. At end of scan of each ADC, they generate separate interrupt request.
ADC Synchronization With The PWM

Traditional Solution

56F801x Solution

PWM Output

PWM Synch signal

ISR Latency

Timer Delay

ADC Convert

Control Algorithm Execution

PWM synch pulse

ADC start signal

ADC Interrupt

PWM values Written to registers

PWM values Updated
A/D Converters
- PWM Synchronization Benefits

- ADC Sampling helps to filtering the measured current - antialiasing.
- Noise free ADC sampling when the power switch is not acting
- ADC sample is taken when Current information is available
56F8000 Digital to Analog Converters

- 12 bit Resolution
- Up to Two independent voltage mode DACs
- 2us settling time settling time when output swing from rail to rail at 3KΩ/400pf load
- Output glitch filter to eliminate switching glitches
- Two output update modes
  - Asynchronous – Update On-demand
  - Synchronous – Update based on PIT or Timer Overflow, or PWM synch signal
- Automatic waveform generation generates square, triangle and sawtooth waveforms with programmable period, update rate, and range
- Software controlled power down mode
56F8000 Analog Comparators

- Up to Two continuous-time differential-input analog comparator modules
- Internal switching matrix supports the independent connection of the analog inputs to the positive or negative input of the analog comparator and to the comparator's export output for another Comparator module.

- 5 selectable Input sources:
  - Three GPIO Pins.
  - One DAC output,
  - One import input from another comparator module
- Programmable comparator output polarity
- Comparator output edge indicator
- Interrupt can be generated by comparator output rising edge, or falling edge, or both edges
- Comparator output can be fed to timer input, PWM faults input, PWM source, external pin output.
- Software controlled power down mode
Analog Comparator Interconnection

- Positive input Source Select: PSEL [0,2]
- Negative input Source Select: NSEL [0,2]
- Source Select: ESEL [0,1]
- Export to CMP_B: MUX
- Import From CMP_B: MUX
- Power Down: PDN
- Programmable Glitch Filter: INV
- Export to CMP_B: CMP_A
- Falling Edge Interrupt Request: COUT
- Rising Edge Interrupt Request: COUT
- To Timer A1: COUT
- To PWM: COUT
- To GPIO: COUT
- To PWM Fault 1: COUT
## Interrupt Priority Structure

### Interrupt Priority Level Summary

<table>
<thead>
<tr>
<th>IPL</th>
<th>Description</th>
<th>Priority</th>
<th>Interrupt Sources</th>
</tr>
</thead>
<tbody>
<tr>
<td>LP</td>
<td>Maskable</td>
<td>Lowest</td>
<td>SWILP Instruction</td>
</tr>
<tr>
<td>0</td>
<td>Maskable</td>
<td>*</td>
<td>On-chip peripherals, IRQA and IRQB, SWI #0 Instruction</td>
</tr>
<tr>
<td>1</td>
<td>Maskable</td>
<td>*</td>
<td>On-chip peripherals, IRQA and IRQB, SWI #1 Instruction</td>
</tr>
<tr>
<td>2</td>
<td>Maskable</td>
<td>*</td>
<td>On-chip peripherals, IRQA and IRQB, SWI #2 Instruction</td>
</tr>
<tr>
<td>3</td>
<td>Non-maskable</td>
<td>Highest</td>
<td>Illegal instruction, hardware stack overflow, SWI instruction, EOnCE Interrupts, misaligned data access</td>
</tr>
</tbody>
</table>

### Current Core Interrupt Priority Levels

<table>
<thead>
<tr>
<th>I1</th>
<th>I0</th>
<th>CCPL</th>
<th>Exceptions Accepted</th>
<th>Exceptions Masked</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>IPL 0,1,2,3, and SWILP</td>
<td>None</td>
<td>This interrupt controller accepts any unmasked interrupt, including the SWILP</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>IPL 1,2,3</td>
<td>IPL 0 and SWILP</td>
<td>This interrupt controller accepts all non-maskable interrupts and any unmasked interrupts that are programmed at level 1 or 2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>2</td>
<td>IPL 2,3</td>
<td>IPL 0, 1 and SWILP</td>
<td>This interrupt controller accepts all non-maskable interrupts and any unmasked interrupts that are programmed at level 1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>3</td>
<td>IPL 3</td>
<td>IPL 0, 1, 2 and SWILP</td>
<td>This interrupt controller only accepts all non-maskable interrupts</td>
</tr>
</tbody>
</table>

* CCPL: Current Core Interrupt Priority Level
Standard Interrupt Arbitration

Interrupt Arbiter

- Illegal Instruction
- SWI #3
- HWS Overflow
- Misaligned Data Access

Priority Level 3 Arbiter

Priority Level 2 Arbiter

Priority Level 1 Arbiter

Priority Level 0 Arbiter

Lowest Priority

Interrupt Request
Vector Table Address
New Interrupt Priority Level

Interrupt Mask Bit

Priority Level Select Bits

If Priority level select Bits is set to 00, the interrupt is disabled

Interrupt Controller

BKPT_U0
TPBUF
IRQA
IRQB
SCI1_RCV

EOOnCE Interrupt Sources

Peripheral Interrupt Sources

- EOOnCE Interrupt Sources can be assigned to priority level 3, 2, and 1.
- Peripheral Interrupt sources can be assigned to priority level 2, 1, and 0.
- Any interrupt sources can interrupt Lowest-Priority Software Interrupt (SWILP interrupt).
Standard Interrupt Processing

**General Case:**
- Vectored Interrupts - Vectors may be located anywhere in Program Memory
- 4 Priority Levels - Highest is non-maskable
- Software Traps at each priority level
- One additional software trap (5th level) at lowest priority for O/S support
The “Fast Interrupt”

**Fast Interrupt Case (Improved latency and throughput):**

- Vectors directly to service routine
- Operates at Interrupt Level 2 - Highest “maskable” priority
- The Frozen PC is copied to FIRA, the status register and NL bit are copied to FISR
- Automatically swaps registers with shadows: R0, R1, N, and M01
- Automatically aligns SP and pushes the Y0 and Y1 registers onto the stack
- Automatically advances the SP to an empty 32-bit location
- Automatically restores above registers on exit, and restores original SP
Read value from A/D into a Circular Buffer in Memory:

Initializing the Fast Interrupt:

- The A/D’s interrupt request is programmed for Level 2 (highest maskable level)
- The shadow registers are initialized:
  - M01 \( \leftarrow \) SIZE - 1
  - R0 \( \leftarrow \) A/D’s memory mapped register
  - R1 \( \leftarrow \) start address in Output Buffer
  - Swap R0, R1, M01 with their shadow registers by using instruction “SWAP SHADOWS”

The Fast Interrupt’s Service Routine:

- The first instruction must not be JSR or BSR
- FRTID is used to return from interrupt (2 delay slots)

```assembly
;Fast Interrupt Service Routine
FRTID ; Return from interrupt - 2 delay slots
MOVE.W X:(R0),Y0 ; Read value from A/D peripheral
MOVE.W Y0,X:(R1)+ ; Write value to circular buffer in memory
```

Total Execution Time: 7 Cycles

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56F8000 Cost Saving

- **56800E architecture optimized for C language**
  - Reduce software development cost
  - Software can be modular and reused

- **On-Chip 12bit Digital-to-Analog Converters (DAC) and Comparators**
  - Dynamic reference settings
  - High speed comparator – Propagation delay: 50ns for internal comparator vs. 1us for external one

- **On-Chip Power-on reset and Low voltage detection**
  - Eliminate external Reset and power supply monitor chip.

- **Single 3.3V supply and 5V I/O port.**
  - Reduce power supply cost
  - Directly interface with 5V system without level shift device

- **On-Chip regulator improves device EMI acceptability**
  - On-Chip 2.5V linear regulator powers the CPU and peripheral logic circuits

- **On-Chip Relaxation oscillator**
  - Eliminate external crystal and reduce PCB size.
  - Greatly improve EMI acceptability

- **Smaller Flash memory page size**
  - Enable User to designate a page flash as EEPROM (eliminate external EEPROM devices)

- **5 Level interrupt priority**
  - Reduce interrupt overhead
  - Improve software efficiency

- **Enhanced On-Chip Emulator**
  - Enable debug of target system using cost effective, isolated debug tool.
**On-Chip Emulator**

- **Host System** *(Windows)*
- **Parallel cable** or **USB cable**
- **JTAG Converter**
- **DSP56800/E Target System**

**Diagram Details**:
- Port IDNT
  - 1A1, 1Y1, 1A2, 1Y2, 1A3, 1Y3, 1A4, 1Y4
  - 2A1, 2Y1, 2Y2, 2A2, 2Y3, 2A3, 2Y4, 2A4
- **51 OHM** resistors
- **3.3V** supply
- **10k ohm** and **1k ohm** resistors
- **74HC244** ICs
- **Reset Switch**
- **/RESET** signal

**Connections**:
- **TMS**, **TCK**, **TDI**, **/TRST**, **TDO**

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Applications
Harm Of Input Harmonics

- Filter capacitance behind the rectifier diodes on in intermission
- Input current aberrance include large number of harmonics
- Sequence: pollute, EMI, interfere etc
Control Method Of PFC Circuit

- **Peak current control**: makes the inductor current follow the reference current. *THD distortion is serious*;
- **Hysteresis current control**: inductor current increases to the upper limit, mosfet off; otherwise, it decreases to the low limit, mosfet on; *simple to control, quick dynamic response, switch frequency changes with duty*.
- **Average current control**: inductor average current follows the reference current. *little current error; little THD and EMI; immune to noise; widely used*. 
Average Current PFC Control

- One Mosfet BOOST PFC circuit is widely used.
- Two main tasks of PFC mission:
  - 1 control inductor current - to make current sinusoidal
  - 2 control output voltage - to insure voltage invariance
Cycle-By-Cycle Controlled PWM

PWM runs at a constant period with pre-set 100% duty cycle. When feedback is greater than reference, the PWM output is truncated (disabled).
Peak current mode control for PFC

Diagram showing the cycle-by-cycle controlled PWM circuit with components labeled as follows:

- LOAD
- RC Filter
- Feedback
- Gate Drive
- COMP
- Reference
- PWM Module
- Fault
- T0
- ANA
- ANB
Power Supply applications
Digital AC to DC Switch mode Power Supply

AC to DC conversion with Power Factor Correction

Isolation

DC to DC conversion using Soft Switching Technology
Interleaving PFC
A/D Converters
- PWM Synchronization Benefits

- ADC Sampling helps to filtering the measured current - antialiasing.
- Noise free ADC sampling when the power switch is not acting
- ADC sample is taken at middle of PWM pulse which is equal to average Current
ADC Synchronization from the PWM Module

56F80xx/83xx

PWM Module

Sync pulse

Primary Clock Source

Timer A3
One Shot Mode

Time delay
ADC Trigger

ADC A

Timer A2
One Shot Mode

Time delay
ADC Trigger

ADC B

PWM Signal

Sync Pulse

Timer Trigger
(Rising Edge Trigger ADC)

Convert anywhere within the PWM cycle
PFC Software Bandwidth

PFC Reload
Interrupt occur
Reload period #1
Reload period #2
Reload period #3

PWM Reload
Interrupt occur

Average input voltage calculation
Current Loop
Display value calculation
Average input current calculation
Current Loop
Display value calculation
Average input voltage calculation
Current Loop
Display value calculation

Voltage Loop

Current Loop

Display value calculation

Voltage Loop

Display value calculation

Current Loop

Display value calculation

Voltage Loop

Display value calculation

Current Loop

Display value calculation

ADC
Phase shifting control

Odd PWM Value Reg
Even PWM Value Reg
Odd PWM Value Reg
Even PWM Value Reg
Odd PWM Value Reg
Even PWM Value Reg

Soft switching operation

PWM Module
Timer A1
One Shot Mode

56F80xx/3xx

T1
T2
T3
T4
T5
T6
TA0
TA1
Vout

V_{AB}
Synchronous Rectification

56F80xx/83xx

PWM Module

Sync pulse

Primary Clock Source

Timer A2
One Shot Mode

PWMs

Timer A0
One Shot Mode

Timer A1
One Shot Mode

V_{AB}

PWM Sync

T1

T2

T3

T4

Start Delay

Reset TA0

Time Delay

Start Delay

Reset TA0

Time Delay

Start Delay

Reset TA0

Time Delay

Reset TA0

Time Delay

Reset TA0

Time Delay

Reset TA0

Time Delay

Reset TA0

Time Delay
Digital controlled isolated DC-DC Converter
DC to DC Software Bandwidth

PWM Reload Interrupt occur

Reload period #1  Reload period #2  Reload period #3

PWM Reload Interrupt

Voltage Loop  Current Loop  Display value calculation
Voltage Loop  Current Loop  Display value calculation
Voltage Loop  Current Loop  Display value calculation

Background Loop

ADC
Hybrid Digital Control

- Voltage Regulator
- Current Regulator
- Digital PWM Module
- Inductor Current Feedback
- Voltage Feedback
- MC56F802x/3x

Slope Compensation

DAC

CMP

Average Current Mode Control

Peak Current Mode Control
Renewable Energy - Solar Panel

DC/DC Booster

Isolated DC/AC Inverter

PWM0 PWM1 ADC0 ADC1

MC56F8013

ADC0 PWM0&1 PWM2&3

MC56F8037

ADC1

MC56F8013
56F8000 Demonstration Kit

- Contents:
  - Demo Board
  - Complimentary permanent license for CodeWarrior® Development Studio with Processor Expert™ tool
  - Utilizes on-chip oscillator
  - JTAG-to-Parallel Port command converter and parallel cable
  - Power supply
  - Preprogrammed sample application
  - Accelerated Development System CD
  - On-board expansion capabilities for development activities
- Ordering Part Number and SRP:
  - DEMO56F8013-EE
  - DEMO56F8014-EE
56F8037 Demonstration Kit

- **Contents:**
  - Demo Board
  - Complimentary permanent license for CodeWarrior® Development Studio with Processor Expert™ tool
  - Utilizes on-chip oscillator (optional off Chip Crystal)
  - USBTAP™ Host Target Interface
  - Addition USB cable to power board via USB port
  - 9V-12V power supply connector
  - Preprogrammed sample application
  - Development System CD
  - On-board 60pin dual row connector expansion capabilities for development activities
  - Ordering Part Number and SRP:
    - MC56F8037EVM
Application Specific Software Libraries

**Memory Manager**
- Dynamic allocation

**Modem Libraries**
- V.8bis, V.21, V.22bis, V.42bis

**Feature Phone Library**
- CallerID type 1 and 2, CallerID Parser, Generic Echo Cancellor

**Security Libraries**
- RSA, DES, 3DES,

**Telephony Libraries**
- AEC, AGC, Caller ID,
- CAS, CPT, CTG, DTMF
- G165, G168, G711
- G723, G726, G729

**Motor Control**
- BLDC, ACIM, SR motor specific algorithms
- General purpose algorithms

**Math Libraries**
- Matrix, Fractional, Vector
- Trigonometric

**Tools Library**
- Cycle Count, FIFO, FileIO, Test

**DSP Library**
- FIR, IIR, FFT, Auto Correlation, Bit Reversal

**Feature Phone Library**
- CallerID type 1 and 2, CallerID Parser, Generic Echo Cancellor

**Security Libraries**
- RSA, DES, 3DES,

**Telephony Libraries**
- AEC, AGC, Caller ID,
- CAS, CPT, CTG, DTMF
- G165, G168, G711
- G723, G726, G729

**Tools Library**
- Cycle Count, FIFO, FileIO, Test
Development Tools - Code Warrior™

CodeWarrior™ Release 8.x for 56800/E
Comprehensive, scalable application development environment allows concurrent approach to hardware, software and system level engineering to minimize time-to-market.

- CodeWarrior™ Development Studio incl. C compiler, assembler, linker, debugger
- New QEDesign Lite filter design tool
- Stand alone Flash programming software
- Processor Expert™ rapid application development (RAD) tool
- Quick Start™ Low level Peripheral Driver provide User Flexibility to Access All Hardware Resources.

- License Pricing:
  - <= 32K bytes FREE license for entire 56F801x/2x Series
  - <= 64K bytes Please contact Freescale Representative
  - <= 128K bytes Please contact Freescale Representative
  - Unlimited Please contact Freescale Representative
Free Filter Design Tool

- Launch QED Filter Design Package.
- Select Equiripple FIR Design, Lowpass.
- Input filter parameters, select Next, get 31 taps, select Next.

This filter has same normalized trans. bandwidth as prior example:
\[ f'_\Delta = 0.0625 \]
\[ N_{\text{taps}} \approx 45 \]

Only need 31 taps because of 1 dB passband ripple
Equiripple (Parks McClellan) FIRs

► Clearly the most popular approach to FIRs
  • Supports arbitrary band shape
  • Filters have equiripple in each passband or stopband

![Graph showing typical amplitude response of an FIR approximation to an ideal lowpass filter.]

*Figure 14.1* Typical amplitude response of an FIR approximation to an ideal lowpass filter.
Filter Design - Graphic Results

- Here’s what you should see:
Filter Design – Coefficients

• Save the coefficients generated.

• Place TestFIRCoefs.h file in Filter Lab project.

• Rebuild filtering project with “new” coefficients. Download and run project.
Why 56F8000?

- **High performance Nonvolatile Memory – Flash memory**
  - Fast access speed, small page size enables user to designate a flash page as EEPROM
  - Longer Data retention and higher program erase cycles
  - Wide operating temperature range (-40°C to 125°C ambient operating temperature)

- **High speed/flexible PWM module**
  - Improved PWM resolution on both duty cycle and frequency – Resonant converter applications
  - Arbitrary PWM pulse generation which can be used for any power stage topology

- **High speed, 12 Analog-to-Digital Converter**
  - High input impedance
  - Various power operating modes

- **High performance On-chip Analog Modules - DACs, Comparators,**
  - Allowing analog designer to work in digital control world
  - Low offset, lifetime drift and gain error
  - Programmable comparator hysteresis
  - Adaptive slope compensation for peak current mode control

- **On-Chip Power-on reset and Low voltage detection**
  - Eliminate external Reset and Power supply monitoring devices.

- **On-Chip regulator improves device EMI acceptability**
  - On-Chip linear regulator powers the CPU and peripheral logic circuits

- **Multiple clock sources – multiple On-Chip clocks and external clock source**
  - Clock redundancy
  - Greatly improve EMI acceptability

- **Enhanced On-Chip Emulator**
  - Enables debugging of target system using low cost, isolated debug tool.

- **5V I/O**
  - Directly Interface to drive circuit

- **Low Cost Development Tool**
  - Enhanced On-Chip Emulator - Enables debugging of target system using low cost, isolated debug tool
  - Free 32KB CodeWarrior License